REMARKS

Upon entry of the present amendment, claim 1 will be amended, whereby claims 1-4 will remain pending. Claim 1 is the sole independent claim.

While not expressing agreement or acquiescence with the rejections of record, claim 1 has been amended to recite "mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made". Support for the amendment to claim 1 appears in Applicants' originally filed application, including the paragraph appearing at page 15, last line to page 16, line 11, and the paragraph appearing at page 25, first full paragraph. Accordingly, no new mater should be considered to be introduced by the present amendment.

Reconsideration of the rejections of record and allowance of the application in view of the following remarks are respectfully requested.

Information Disclosure Statement

Applicants express appreciation for the inclusion with the Office Action of a completely initialed Form PTO-1449 including the confirmation of consideration of JP 2000-196197.

Response To Rejections

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being unpatentable over U.S. Patent No. 6,333,522 to Inoue et al. (hereinafter "Inoue") in view of U.S. Patent Publication No. 2003/0160258 to Oohata.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue and Oohata, and further in view of U.S. Patent No. 6,878,973 to Lowery et al. (hereinafter "Lowery").

In response to these grounds of rejection, Applicants submit that none of the documents of record teaches or suggests, as recited in Applicants' independent claim 1, a light-emitting device formed by depositing p-type and n-type nitride semiconductor layers, comprising:

deposited p-type and n-type nitride semiconductor layers;

semiconductor-surface-electrodes to apply currents into each of the semiconductor layers;

an insulating layer which holds the semiconductor layers, said insulating layer comprising two surfaces; and

mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made;

wherein one of the semiconductor layers has a non-deposited area where the other semiconductor layer is not deposited;

one of the semiconductor-surface-electrodes is built up on the surface of the non-deposited area;

vias are made in the insulating layer which electrically connect the semiconductor-surface-electrodes and the mount-surface-electrodes;

the semiconductor-surface-electrodes, the insulating layer, and the mount-surface-electrodes are built up in this order on one side of the deposited semiconductor layers; and

a surface of the other side of the deposited semiconductor layers is a light emitting surface which emits light beams directly to outside from the semiconductor layers.

Applicants submit that the any combination of the prior art, even if the prior art is properly combinable, does not teach or suggest Applicants' recited subject matter which includes, amongst other features set forth in the recited combinations, mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made. In this regard, the Examiner's attention is directed to the paragraph appearing at page 15, last line to page 16, line 11 of Applicants' specification, wherein it is disclosed that:

> With such a configuration, the light-emitting device 1 comprises mount-surface-electrodes 5 on the surface opposite the light-emitting surface, and because of this fact, the light-emitting device 1 can be treated as a surface-mount device which is mounted on a print-circuit board, and the mounting method used for the print-circuit board can be applied for the mounting of the light-emitting device. This means that the semiconductor mount technologies such as wire-bonding, flip-chip-bonding, or the like are not required, and the surface mount technologies such as solder re-flow, or the like can be utilized. Furthermore, since the light extraction surface of the light-emitting device 1 is not covered by transparent crystal substrate such as sapphire, light beams can be extracted directly and efficiently to outside from the semiconductor layers 2, 3.

Moreover, it is disclosed at the paragraph appearing at page 25, first full paragraph, of Applicants' specification, that:

> As another filling method for VIA holes 41, as shown FIG. 10A and FIG. 10B, a method using solder is available, where the solder is used for mounting the device onto mounting substrate 54. The thermal conductivity of the solder is, for example, 50 W/m/K, and solder can efficiently dissipate the heat. For the mounting of the light-emitting device, the device mounting process in the print-circuit board technologies can be used, and therefore no special mounting process is necessary, and the mounting process can be made simple too.

Thus, it is readily apparent from Applicants' application as originally filed that the mount-surface-electrodes are structured and arranged to mount the light-emitting device onto a mounting substrate by using solder.

In contrast to the subject matter recited in Applicants' independent claim 1, and further defined in the dependent claims, Inoue does not teach or suggest a light-emitting device including, amongst the combination of features, mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder. The light-emitting device disclosed by Inoue is structured and arranged for microbump mounting, as see, for example, the Abstract of Inoue.

Moreover, Oohata does not overcome the deficiencies of Inoue. Thus, whether or not one having ordinary skill in the art would have made the asserted combination of Inoue and Oohata, which Applicants submit would not have been made, such combination does not overcome the above-discussed differences over Inoue. The light-emitting devices disclosed by Oohata are devices for an image display system, and the devices are arranged in a matrix and covered by an insulating layer, and electrically connected by vias and wirings, as see, for example, Figs. 38 and 39 and the associated disclosure in paragraph [0106] of Oohata.

Therefore, the rejection of claim 1-3 is without appropriate basis at least for the reasons set forth above, and should be withdrawn.

Regarding the obviousness rejection of claim 4, Lowery is merely utilized in the rejection in an attempt to establish obviousness of including phosphor on the surface of the semiconductor layer. However, whether or not one having ordinary skill in the art would have made the asserted combination of Inoue, Oohata and Lowery, which Applicants submit would not have been made, such combination does not overcome at least the above-discussed differences over

the asserted combination of Inoue and Oohata. Therefore, the rejection of claim 4 is without appropriate basis, and should be withdrawn.

Accordingly, each of the rejections of record should be withdrawn, and the application should be allowed

CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections of record, and allow each of the pending claims.

Applicants therefore respectfully request that an early indication of allowance of the application be indicated by the mailing of the Notices of Allowance and Allowability.

Should the Examiner have any questions regarding this application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
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